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| 10/038,546 | 10/24/2001 | Alexander I. Krymski | 08305-118001 | 7123 |

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| EXAMINER | |
|---|---|
| QUIETT, CARRAMAH J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2612 | |

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,546 | KRYMSKI, ALEXANDER I. | |
| | Examiner | Art Unit | |
| | Carramah J. Quiett | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4,6-26 and 28-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-26, and 28-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. The amendment(s), filed on 1/28/2005, have been entered and made of record. Claims 1-4, 6-26 and 28-30 are pending. The Applicant has canceled claims 5 and 27.

### *Response to Arguments*

2. Applicant's arguments with respect to **claims 1-30** have been considered but are moot in view of the new ground(s) of rejection.

In order to overcome the amendments to independent claims 1, 13, and 25, the examiner has combined Miura and Numazaki, the references used in the prior Office Action (dated 11-03-2004), into a 35 USC 103(a) rejection. However, the applicant traverses the combination of these references. The examiner respectfully disagrees.

Miura has been used to teach all of the limitations in independent claims 1, 13, and 25 *except* for the following limitations highlighted in italics:

> Claim 1 – (iv) a first switchable element for electrically coupling an output of said photosensitive element with said first capacitive element *during a first integration period*, and (v) a second switchable element for electrically coupling an output of said photosensitive element with said second capacitive element *during a second integration period.*

Claim 13 – a controller configured for providing signals to control the selective coupling of the first and second capacitive storage elements and the photosensitive element *during a respective first and second integration period* of the pixel.

Claim 25 – a method comprising: storing a first signal level, sensed by a photosensitive element *during a first integration period* and storing a second signal level, sensed by the photosensitive element *during a second integration period.*

In order to overcome the limitations that Miura does not expressly teach, the examiner has included Numazaki. As stated earlier, the applicant transverses the combination of this reference. The applicant argues that:

a. The statement made by the examiner, in the prior Office Action, regarding the timing controller is neither taught nor suggested by Numazaki and that the examiner has applied impermissible hindsight when considering the claimed invention.

b. Numazaki does not teach or suggest "a first switchable element for electrically coupling an output of said photosensitive element with said first capacitive element during a first integration period, and a second switchable element for electrically coupling an output of said photosensitive element with said second capacitive element during a second integration period."

c. Integration periods are not considered in the Numazaki reference.

d. Numazaki does not teach the internal accumulation of charges associated with first and second integration periods of a pixel cell, as in the claimed invention.

Once again, the examiner respectfully disagrees. The examiner has not applied impermissible hindsight. The timing controller is configured for providing signals to cause the first capacitive

storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time.

Numazaki discloses and illustrates a timing controller in figs. 1-2, refs. 9/18 and col. 3, lines 40-43. Then, in col. 3, lines 45-50, Numazaki teaches that his image detecting section is similar the image-capture elements of a CCD. The primary reference, Miura, provides an example of driving an image pick-up unit with a CCD. Numazaki expounds on the capabilities of the CCD by including a mechanism configured to separate reflect light from external light and taking out the reflected light (Numazaki, col. 3, lines 45-58). The secondary reference, Numazaki has been used to teach the driving of a CCD during a first integration period and a second integration period. As well known in the art, charges accumulate in (or are added to) the CCD when exposed to light for a period of time. Numazaki has a timer for controlling his image detecting section (col. 3, lines 45-50). The term "integration" is a synonym for the term "accumulation." Miura teaches integration period by explaining the expounding on the circuitry (Miura, figs. 16-17) and Numazaki explains two integration periods (Numazaki, col. 3, lines 45-58).

Miura and Numazaki will be combined to reject claims 2-4, 6-12, 14-26, and 28-30, under 35 USC 103(a), as well.

### *Claim Rejections - 35 USC § 103*

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claims 1-4, 6-26, 28-30** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura (U.S. #6,501,506) in view of Numazaki et al. (U.S. #6,628, 335).

As for **claim 1**, Miura discloses an apparatus (fig. 16, seventh mode of implementation) comprising:

a pixel (fig. 16) including (i) a buffer transistor (ref. 8) having an input, (ii) first (ref. 12b) and second (ref. 12a) capacitive storage elements each of which selectively can be coupled to the input of the buffer transistor (via sample and hold transistors 10b and 10a, respectively), (iii) a photosensitive element (ref. 2) having an output which selectively can be coupled to the input of the buffer transistor via transfer transistor (ref. 4) (col. 10, line 64 – col. 11, line 14), and (iv) a first switchable element (10b) for electrically coupling an output of said photosensitive element with said first capacitive element (12b), and (v) a second switchable element (10a) for electrically coupling an output of said photosensitive element with said second capacitive element (12a) (col. 10, line 64 – col. 11, line 14). Additionally, in Miura's disclosure, charges are stored in the first and second capacitive elements (fig. 16, ref. 12b and 12a, respectively) connected in parallel and subsequently read out two times. Miura also states that the timing of the signal storage period can be generated by an externally provided timing circuit and by timing the reading by an internally provided timing circuit. Please read column 12, lines 30-35; and

a readout circuit (refs. 60, 72, 52) that selectively can be coupled to an output of the buffer transistor (col. 11, lines 8-14 and 30-36). Also, please read column 1, lines 21-28 and column 11, lines 17-36.

However, Miura does not expressly disclose (iv) a first switchable element for electrically coupling an output of said photosensitive element with said first capacitive element

*during a first integration period*, and (v) a second switchable element for electrically coupling an output of said photosensitive element with said second capacitive element *during a second integration period*;

In the same field of endeavor, Numazaki teaches an image capturing apparatus (col. 3, lines 41-43) where the timing controller (fig. 1, ref. 9) controls the operation of the image detecting section (fig. 1, ref. 4). The cell (ref. 15) of image detecting section, illustrated in figure 2, comprises an accumulation control section (ref. 11) that controls where the image signal of the photoelectric converter section should be accumulated. Signals are accumulated in the first and second charge accumulating sections (refs. 12 and 13). This means that the timing controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66. In light of the teaching of Numazaki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miura's circuit with a first switchable element for electrically coupling an output of said photosensitive element with said first capacitive element during a first integration period, and a second switchable element for electrically coupling an output of said photosensitive element with said second capacitive element during a second integration period in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

For **claim 2**, Miura, as modified by Numazaki, discloses an apparatus including: a first switch (ref. 4) coupled between the output of the photosensitive element and the input of the

buffer transistor, and wherein the first switchable element (ref. 10b) is a second switch coupled between the first capacitive storage element and the input of the buffer transistor and the second switchable element (ref. 10a) is a third switch coupled between the second capacitive storage element and the input of the buffer transistor, each of the switches being selectively operable in an open or closed state. Also, please read column 10, lines 66-67 and column 11, lines 1-13.

As for **claim 3**, Miura, as modified by Numazaki, discloses an apparatus including a fourth switch (fig. 16, ref. 6) coupled between a power supply node and the input of the buffer transistor, the fourth switch being selectively operable in an open or closed state. Also in figure 16, the fourth switch (ref. 6) is connected to a power supply node via potential of wire 42. In fact, the fourth switch can be turned on (closed) (col. 11, lines 17-18). Therefore, it can be turned off (opened) as well.

As for **claim 4**, Miura, as modified by Numazaki, discloses an apparatus including a controller configured for providing signals to control the respective states of the first, second, third and fourth switches. In figure 16, Miura illustrates control lines 92, 96, and 98 from the vertical shift register (ref. 60) for controlling the fourth (ref. 6), second (ref. 10b), and third (10a) switches, respectively (col. 10, line 66-67; col. 11, lines 1-13). The first switch (ref. 4) is controlled by a TRANSFER signal, which turns it on or off (col. 11, lines 60-64).

As for **claim 6**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing signals to cause (i) the first and second switches to be closed during the first integration time, (ii) the third and fourth switches to be open during the first integration time, (iii) the first and third switches to be closed during the second integration time, and (iv) the second and fourth switches to be open during the second integration time.

Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference # 4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. Miura teaches that after the potential of the wiring is returned to its original high potential, the charges are injected into the first and second sample and hold capacitors. According to the structure of the circuit diagram illustrated in figure 16, it is imperative for the first and second switches to be on during the first integration time, the third and fourth switches to be off during the first integration time, so that the charges can be injected into only the first capacitor without resetting. Similarly, it is also imperative, according to the structure of the circuit diagram in figure 16, for the first and third switches to be on during the second integration time and the second and fourth switches to be off during the second integration time, so that the charges can be injected into only the second capacitor without resetting.

As for **claim 7**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing signals to cause (i) the first, second and fourth switches to be closed just prior to the first integration period, and (ii) the first, third and fourth switches to be closed just prior to the second integration period. Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference # 4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. According to the structure of the circuit diagram illustrated in figure 16, Miura's circuit to performs the limitations listed above so that only one storage capacitor can reset one at a time and so that the charging process can be complete before the next one begins.

As for **claim 8**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing capacitive storage element prior to the second integration period signals to reset the photosensitive element and the first capacitive storage element prior to the first integration period and to reset the photosensitive element and the second. Referring to the figure 16 of Miura, please note that Examiner considers the first switch to be reference #4, the second switch to be reference #10b, the third switch to be reference #10a, and the fourth switch to be reference #6. Please read column 10, line 66-67 and column 11, lines 1-13 and lines 60-64. According to the structure of the circuit diagram illustrated in figure 16, it is imperative for Miura's circuit to perform the limitations listed above so that the charging process can be complete before the next one begins.

As for **claim 9**, Miura discloses an apparatus wherein the controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element and to cause the second capacitive element to store a second signal level sensed by the photosensitive element. Please read column 11, lines 17-36. However, Miura does not explicitly disclose a controller configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive storage element to the readout circuit. His disclosure states that the corresponding components of his circuit are selected for signal charges to be stored in the first and second storage capacitors.

Numazaki discloses an image capturing apparatus (col. 3, lines 41-43) a timing controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the

second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66. His timing controller is further configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive storage element to the readout circuit. His disclosure states that the corresponding components of his circuit are selected for signal charges to be stored in the first and second storage capacitors. Numazaki has an output section that selects either the fist charge accumulating section or the second charge accumulating section and reads its electric charge to the outside of the cell. Please read column 3, lines 59-67 and column 4, lines 1-2.

Furthermore, in Miura's disclosure, charges are stored in the first and second capacitive elements (fig. 16, ref. 12b and 12a, respectively) connected in parallel and subsequently read out two times. Miura also states that the timing of the signal storage period can be generated by an externally provided timing circuit and by timing the reading by an internally provided timing circuit. Please read column 12, lines 30-35. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the limitations of claim 9 with the image pick-up device of Miura in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

As for **claim 10**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing signals to reset the input of the buffer transistor (fig. 16, ref. 8) prior to transferring the first signal level from the first capacitive storage element (fig. 16, 10b) to the readout circuit and to reset the input of the buffer transistor prior to transferring the

second signal level from the second capacitive storage element (fig. 16, 10a) to the readout circuit. According to the structure of the circuit diagram illustrated in figure 16, it is imperative for Miura's circuit to perform the limitations listed above so that the charging process can be complete before the next one begins. Please refer to the rejection for claim 9 for the reasons for obviousness.

As for **claim 11**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing signals to cause the fourth switch to be closed prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to cause the fourth switch to be closed just prior to transferring the second signal level from the second capacitive storage element to the readout circuit. According to the structure of the circuit diagram illustrated in figure 16, it is imperative for Miura's circuit to perform the limitations listed above so that the charging process can be complete before the next one begins.

As for **claim 12**, Miura, as modified by Numazaki, discloses an apparatus wherein the fourth switch is configured for operation in a sub-threshold reset mode. As stated in Miura's disclosure and illustrated in figure 16, the reset transistor (ref. 6) and the sample hold transistors (refs. 10a, 10b) are turned on and the potential of the wiring 42 is set low (col. 11, lines17-19) as well as adjusting the variation in the threshold value (col. 11, 45-46).

As for **claim 13**, Miura discloses an apparatus (in the seventh mode of implementation of his solid state pick-up unit in figure 16) comprising:

an array of pixels each of which is associated with a respective row and column in the array, each pixel, as shown in figure 1, including (i) a buffer transistor (ref. 8) having an input, (ii) first (ref. 12b) and second (ref. 12a) capacitive storage elements each of which selectively

can be coupled to the input of the buffer transistor (via sample and hold transistors 10a and 10b), respectively, and (iii) a photosensitive element (ref. 2) having an output which selectively can be coupled to the input of the buffer transistor via transfer transistor 4;

readout circuitry (refs. 60, 72, 52) which selectively can be coupled to outputs of buffer transistors of selected pixels in the array (col. 11, lines 8-14 and 30-36); and

a controller configured for providing signals to control the selective coupling of the first (ref. 12b) and second (ref. 12a) capacitive storage elements and the photosensitive element (ref. 2) of the pixel. In figure 16, Miura illustrates control lines 96 and 98 from the vertical shift register (ref. 60) for controlling the first (ref. 12b) and second (ref. 12a) capacitive storage elements via the second (ref. 10b), and third (ref. 10a) switches, respectively (col. 11, lines 8-13). Additionally, the photosensitive element (ref. 2) to the input of the buffer (ref. 8) is controlled by a TRANSFER signal via the fourth switch (ref. 4), which turns it on or off (col. 11, lines 60-64). However, Miura does not expressly disclose a controller configured for providing signals to control the selective coupling of the first and second capacitive storage elements and the photosensitive element *during a respective first and second integration period* of the pixel.

In the same field of endeavor, Numazaki teaches an image capturing apparatus (col. 3, lines 41-43) where the timing controller (fig. 1, ref. 9) controls the operation of the image detecting section (fig. 1, ref. 4). The cell (ref. 15) of image detecting section, illustrated in figure 2, comprises an accumulation control section (ref. 11) that controls where the image signal of the photoelectric converter section should be accumulated. Signals are accumulated in the first and second charge accumulating sections (refs. 12 and 13). This means that the timing controller is configured for providing signals to cause the first capacitive storage element to store a first

signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66. In light of the teaching of Numazaki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miura's circuit with a controller configured for providing signals to control the selective coupling of the first and second capacitive storage elements and the photosensitive element (ref. 2) during a respective first and second integration period of the pixel in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

For **claim 14**, Miura, as modified by Numazaki, discloses an apparatus including: a first switch (ref. 4) coupled between the output of the photosensitive element and the input of the buffer transistor, and wherein is a second switch (ref. 10b) coupled between the first capacitive storage element and the input of the buffer transistor and a third switch (ref. 10a) coupled between the second capacitive storage element and the input of the buffer transistor, each of the switches being selectively operable in an open or closed state. Also, please read column 10, lines 66-67 and column 11, lines 1-13.

**Claims 15-16** are integrated circuit claims and are written similar for claims 3-4. Please read the rejections for claims 3-4 for the reasons for rejecting claims 15-16, respectively.

For **claim 17**, Miura, as modified by Numazaki, discloses an apparatus wherein the controller is configured for providing signals to control the selective coupling of the readout circuitry (refs. 60, 72, 52) to the outputs of the buffer transistors (col. 11, lines 8--36).

**Claims 18-24** are an integrated circuit claims and is written similar for claims 6-12, respectively. Please read the rejection for claims 6-12 for the reasons for rejecting claims 18-24, respectively.

As for **claim 25**, Miura discloses a method comprising:

storing a first signal level, sensed by a photosensitive element in a first capacitive storage element in a pixel (column 12, lines 30-35);

storing a second signal level, sensed by the photosensitive element in a second capacitive storage element in the pixel (column 12, lines 30-35); and

reading out the first and second signal levels from the pixel (col. 11, lines 8-14 and 30-36). Also, please read column 1, lines 21-28 and column 11, lines 17-36. However, Miura does not expressly teach a method for storing a first signal level, sensed by a photosensitive element during a first integration period and storing a second signal level, sensed by the photosensitive element during a second integration period.

In the same field of endeavor, Numazaki teaches an image capturing apparatus (col. 3, lines 41-43) where the timing controller (fig. 1, ref. 9) controls the operation of the image detecting section (fig. 1, ref. 4). The cell (ref. 15) of image detecting section, illustrated in figure 2, comprises an accumulation control section (ref. 11) that controls where the image signal of the photoelectric converter section should be accumulated. Signals are accumulated in the first and second charge accumulating sections (refs. 12 and 13). This means that the timing controller is configured for providing signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element

during a second integration time. Please read column 1, lines 26-37 and column 3, lines 45-66. In light of the teaching of Numazaki, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miura's circuit with a method for storing a first signal level, sensed by a photosensitive element during a first integration period, in a first capacitive storage element in a pixel and storing a second signal level, sensed by the photosensitive element during a second integration period in order to provide an image capture module for inputting a shape of an object on a three-dimensional space (Numazaki, col. 1, lines 45-47).

As for **claim 26**, Miura, as modified by Numazaki, teaches a method including obtaining a signal representing the difference between the first and second signal levels read from the pixel in column 11, lines 30-36.

**Claims 28 and 29** are method claims corresponding to claims 8 and 10, respectively. Please read the rejection for claims 28 and 29 for the reasons for rejecting claims 8 and 10, respectively.

As for **claim 30**, Miura, as modified by Numazaki, teaches a method including operating a pixel reset switch in a sub-threshold reset mode. As stated in Miura's disclosure and illustrated in figure 16, the reset transistor (ref. 6) and the sample hold transistors (refs. 10a, 10b) are turned on and the potential of the wiring 42 is set low (col. 11, lines17-19) as well as adjusting the variation in the threshold value (col. 11, 45-46). Furthermore, claim 30 is dependent on claim 28. Please read the rejection for claim 28 for the reasons for obviousness in view of Numazaki et al.

***Conclusion***

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent Application Publication

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|---|---|
| Lee, Won-Ho (2004/0218078) | CMOS image sensor with two transfer transistors for transferring the stored charges in the photodiode (see fig. 4 and page 2, paragraphs 26-34). |

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (571) 272-7316. The examiner can normally be reached on 8:00-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (571) 272-7308. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.J.Q.
July 27, 2005

NGOC-YEN VU
PRIMARY EXAMINER